FORM PTO-1390
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

EXPRESS MAIL LABEL NO.: EL 388 784 122 US

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US)

CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: Furusawa Case 49

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): Unknown

INTERNATIONAL APPLICATION NO.: PCT/JP98/03317 INTERNATIONAL FILING DATE: July 24, 1998

PRIORITY DATE CLAIMED: July 25, 1997

TITLE OF INVENTION: CONTOUR EMPHASIZING CIRCUIT

APPLICANTS FOR DO/EO/US: (1) Toru AIDA, (2) Seiji MATSUNAGA and (3) Junichi ONODERA

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [X] This express request to begin national examination procedures (35 U.S.C. 371(f) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. [X] A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [] is transmitted herewith (required only if not transmitted by the International Bureau).
   b. [X] has been transmitted by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. [ ] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. [ ] are transmitted herewith (required only if not transmitted by the International Bureau).
   b. [ ] have been transmitted by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. [ ] A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [X] A FIRST preliminary amendment.
    [ ] A SECOND or SUBSEQUENT preliminary amendment.
14. [ ] A substitute specification.
15. [ ] A change of power of attorney and/or address letter.
16. [X] Other items or information:
    Amendment Before First Office Action
    Formal Drawings (3 sheets)
    Title Page of WIPO Document WO99/05855
    Postal Card

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U.S. APPLICATION NO. (if know, see 37 CFR 1.5): Unknown

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428 Rec'd PCT/PTO 24 JAN 2000

09/463642

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17. [X] The following fees are submitted:

CALCULATIONS PTO USE ONLY

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)):

Search Report has been prepared by the EPO or JPO ..... $ 840.00
International preliminary examination fee paid to USPTO (37 CFR 1.482)..... $ 670.00
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2))..... $ 690.00
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO..... $ 970.00
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) .... $ 96.00

ENTER APPROPRIATE BASIC FEE AMOUNT = $840.00

Surcharge of $130.00 for furnishing the oath or declaration later than [] 20 [] 30 months from the earliest claimed priority date (37 CFR 1.492(e)). $

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	4 - 20 =	0	X $ 18.00	$
Ind. claims	1- 3 =	0	X $ 78.00	$
MULTIPLE DEPENDENT CLAIMS (if applicable)			+ $260.00	$
TOTAL OF ABOVE CALCULATIONS			=	$840.00
Reduction by 1/2 for filing by small entity, if applicable. Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28).			-	$
SUBTOTAL			=	$840.00
Processing fee of $130.00 for furnishing the English translation later than [] 20 [] 30 months from the earliest claimed priority date (37 CFR 1.492(f)).			+	$
TOTAL NATIONAL FEE			=	$840.00
Fee for recording assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property			+	$
TOTAL FEES ENCLOSED			=	$840.00
Amount to be refunded				$
charged				$

a. [X] A check in the amount of $840.00 to cover the above fees is enclosed.
b. [ ] Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.
c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 06-1382. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

IN DUPLICATE

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IN THE U.S. PATENT AND TRADEMARK OFFICE

January 24, 2000

Applicants : Toru AIDA et al

For : CONTOUR EMPHASIZING CIRCUIT

PCT International Application No.: PCT/JP98/03317

PCT International Filing Date: July 24, 1998

U.S. Application No.
(if known, see 37 CFR 1.5): Unknown

Atty. Docket No.: Furusawa Case 49

Box PCT
Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT CANCELLING CLAIMS

Sir:

Prior to calculation of the filing fee in the above-identified application, kindly enter the following:

IN THE CLAIMS

Please amend Claim 4 as follows.

Claim 4, line 1; delete "2 or 3".

REMARKS

This amendment cancels claims to reduce the filing fee. Please enter this amendment before calculating the filing fee.

Respectfully submitted,

Terryence F. Chapman

TFC/smd

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Encl: None

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Washington, DC 20231

AMENDMENT BEFORE FIRST OFFICE ACTION

Sir:

Prior to issuance of the first Office Action in the above-identified application, kindly enter the following:

IN THE CLAIMS

Please cancel Claims 1-4 and replace them with newly presented Claims 5-9 as follows.

5. A contour emphasizing circuit comprising a contour pick-up unit for sampling contour component from input video signal, a level judging unit comprising a decoder for dividing the luminance level into n number (n = integers between 2 m-1~2m) of levels by discriminating the luminance level of the input video signal on the basis of m-bit data of upper luminance levels, a coefficient control unit for selectively changing coefficient among n number of coefficients, that is, selecting a high-value coefficient for a high luminance level and a low-value coefficient for a low luminance level, according to judging signal from the level judging unit to

multiply the contour component sampled by means of the contour pick-up unit for outputting the product thereof, and an adder for adding the contour component output from the coefficient control unit to the input video signal for outputting a contour-emphasized video signal.

6. A contour emphasizing circuit according to Claim 5, wherein the coefficient control unit comprises n number of multipliers for multiplying the contour component sampled by using the contour pick-up unit by the coefficient corresponding to one of said n number of luminance levels for outputting the product thereof, n number of AND gates respectively connected to the output sides of the n number of multipliers for using the signal interpreted by said decoder as gate control signal, and an OR gate connected to the output sides of the n number of AND gates.

7. A contour emphasizing circuit according to Claim 5, wherein the level judging unit comprises a decoder for discriminating the luminance level of an input video signal on the basis of m-bit data of upper luminance levels to divide the luminance level into n number (n = 2 m-1) of luminance levels, whose maximum values range from 1 or less, 1/2 or more, 1/2 or less, 1/4 or more, 1/4 or less, 1/8 or more, ..., to 0 or more, to interpret whether the luminance level of an input video signal corresponds to which of the n number of luminance levels.

8. A contour emphasizing circuit according to Claim 7, wherein the level judging unit comprises the decoder for interpreting whether the luminance level of input video signal corresponds to which of four luminance levels, and the coefficient control unit comprises four multipliers for multiplying the contour components sampled by using the

contour pick-up unit by any of coefficients 1/8, 1/4, 1/2 and 1 for outputting the product thereof, four AND gates respectively connected to the output sides of the four multipliers for using the signal interpreted by said decoder as gate control signal, the OR gate connected to the output sides of the four AND gates.

9. A contour emphasizing circuit according to Claim 5, wherein the contour pick-up unit comprises a horizontal contour component pick-up unit for sampling the contour component in horizontal direction from input video signal.

REMARKS

Entry of the foregoing amendments prior to issuance of the first Office Action is respectfully solicited. These amendments incorporate the Article 34.2(b) amendments made to the claims at the PCT level and are intended to place the application in better form for consideration by the Examiner.

Respectfully submitted,

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Encl: None

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SPECIFICATION

CONTOUR EMPHASIZING CIRCUIT

TECHNICAL FIELD

The present invention relates to a contour emphasizing circuit designed for sampling contour component from input video signal (e.g., digital input video signal), multiplying the sampled contour component by a coefficient (one of coefficients including 1) for contour emphasis, and adding the product thereof to the input video signal for outputting contour-emphasized video signal.

BACKGROUND OF THE INVENTION

The PDP (Plasma Display Panel) equipment using the plasma display panel and LCD (Liquid Crystal Display) equipment using the liquid crystal display panel as thin and lightweight display equipment have come to attract public attention. Such display equipment is conventionally of direct-drive type using digital video signal, wherein a contour emphasizing circuit, such as one shown in Fig. 1, is used for obtaining the contour-emphasized video signal from the input video signal.

The contour emphasizing circuit shown in Fig. 1 comprises a contour pick-up unit 10, a delay adjusting unit 12 and adder 14.

The contour pick-up unit 10 comprises one-dot delay units 18, 20 for sequentially delaying by one-dot the digital luminance signals (an example of video signal), which has been input to the input terminal 16, adder 22 for adding the luminance signal Y input to the input terminal 16 to the output signal from the one-dot terminal 16 to obtain the sum, multiplier 26 for multiplying the sum by coefficient 1/4 for outputting the product thereof, a multiplier 26 for multiplying the output signal from the one-dot delay unit 18 by coefficient 1/2 for outputting the product thereof, and a subtracter 28 for subtracting the output signal of

the multiplier 24 from the output signal of the multiplier 26; wherein the contour component (i.e., high-pass component) HE in horizontal direction of reference picture element are sampled, for output, from the picture elements on the left side and right side (preceding and subsequent picture elements on time basis) of the reference picture element.

A delay adjusting unit 12 is designed for adjusting the timing for the input of the luminance signal, which has been input to the input terminal 16, to the adder 14 to the timing for the input of the contour component HE, which has been sampled by contour pick-up unit 10, to the adder 14 by delaying the output of luminance signal Y, which has been input to the input terminal 16, for a predetermined time interval.

The adder 14 adds the luminance signal Y, which is output from the delay adjusting unit 12, to the contour component HE, which is sampled the contour pick-up unit 10, to output the sum (Y + HE), as a contour-emphasized component, to an output terminal 30.

However, the contour emphasizing circuit shown in Fig. 1 has a problem as is described below because of being designed so that the contour component HE sampled by the contour pick-up unit 10 is directly output to the adder 14 regardless of the luminance level of the luminance signal Y input to the input terminal 16 is high or low.

The problem is that unnatural picture having overemphasized contour is produced if a contour component having too high a value is added to a relatively dark picture of a low luminance level. Another problem of the circuit is that the contour cannot be emphasized sufficiently if a contour component having to low a value is added to a bright picture having a high luminance level.

The present invention is designed for the purposes of solving the above problems and for providing a contour emphasizing circuit capable of accomplishing contour emphasis matching the luminance level of input video signal.

DISCLOSURE OF THE INVENTION

The contour emphasizing circuit according to the present invention is characterized by

comprising a contour pick-up unit for sampling contour component from input video signal, a luminance level judging unit for discriminating the luminance level of input video signal, a coefficient control unit for not only selectively changing coefficient among a plurality of coefficients according to the judging signal from the luminance level judging unit but also multiplying the contour component sampled by means of a contour pick-up unit by a selected coefficient for the outputting the product thereof and an adder for adding the contour component output from the coefficient control unit to input video signal for outputting contour-emphasized video signal.

A coefficient is selected from among a plurality of coefficients, so that a plurality of coefficients are available for being multiplied by the contour component according to the luminance level of the input video signal. Thus, the picture can be prevented from becoming unnatural picture by controlling the contour component to be added to the input video signal to a value matching the luminance level of the input video signal.

Further, the level judging unit may comprise a decoder for discriminating the luminance level of the input video signal from among n number (n = 2 and larger integers) of luminance levels, and the coefficient control unit may comprise n number of multipliers for multiplying the contour component, which is sampled by means of the contour pick-up unit, by the coefficient corresponding to each luminance level among n number of luminance levels for outputting the product thereof, n number of AND gates using, as the gate control signal, the signal interpreted by the decoders connected respectively to the output sides of the n number of multipliers and an OR gate connected to the output sides of the n number of the AND gates. By doing so, the level judging unit and the coefficient control unit can be formed easily.

Further, the level judging unit may comprise a decoder capable of discriminating each of 4 luminance levels of input video signal, and the coefficient control unit may comprise 4 multipliers for multiplying the contour component, which is sampled by the contour pick-up unit, by one of the coefficients 1/8, 1/4, 1/2 and 1 for outputting the product thereof, 4 AND

gates respectively connected to the output sides of the 4 multipliers for using, as the gate control signal, the signal interpreted by the decoders respectively connected, and an OR gate connected to the output side of the 4 AND gates. By doing so, the level judging unit and the coefficient control unit can be formed more easily.

Further, the composition of the contour pick-up unit can be simplified by composing the contour pick-up unit with a horizontal contour component pick-up unit designed for sampling the contour component in horizontal direction from input video signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing an example of conventional contour emphasizing circuit.

Fig. 2 is a block diagram showing an embodiment of the contour emphasizing circuit according to the present invention.

Fig. 3 is a block diagram showing examples of the level judging unit and the coefficient control unit shown in Fig. 2.

BEST MODES FOR CARRYING OUT THE PRESENT INVENTION

The content of the present invention will be described in detail referring to the accompanying drawings.

Fig. 2 shows a contour emphasizing circuit as an embodiment of the present invention, wherein common reference numerals are assigned to those parts common to those shown in Fig. 1.

In Fig. 2, numeral 10 denotes the contour pick-up unit; 12,13, the delay adjusting unit; 14, an adder; 15, the level judging unit; 17, coefficient control unit.

The contour pick-up unit 10 comprises one-dot delay units 18, 20 for sequentially delaying by 1 dot the digital luminance signals (an example of video signal), which has been input to the input terminal 16, adder 22 for adding the luminance signal Y input to the input

terminal 16 to the output signal from the one-dot terminal 16 to obtain the sum, multiplier 26 for multiplying the sum by coefficient 1/4 for outputting the product thereof, and subtracter 28 for subtracting the output signal of the multiplier 24 from the output signal of the multiplier 26; wherein the contour components HE in horizontal direction are sampled, for output, from the picture elements on the left side and right side of the reference picture element.

The level judging unit 15 is designed to discriminate the luminance level of the luminance signal Y input to said input terminal 16 and output a corresponding judging signal. More specifically, as shown in Fig. 3, (the level judging unit 15) comprises the decoder 32 for decoding the luminance level of the luminance signal Y with reference to the values of the upper 3 bits

of the 8-bit luminance signal Y. That is, the decoder 32 outputs a signal (e.g., H-level signal) corresponding to the output sides ①, ②, ③ and ④ depending on whether the values of the upper 3 bits of the luminance signal Y input to the input terminal 16 correspond to which of [000], [001], [010~011] and [100~111], thereby interpreting whether the luminance level of the luminance signal Y corresponds to which of the hexadecimal numbers of 4 levels, namely, [00~1F], [20~3F], [40~7F] and [80~FF].

The coefficient control unit 17 is designed for selectively changing the coefficient according to the judging signal output from the level judging unit 15 by way of the delay adjusting unit 13, as well as for multiplying the contour component sampled by means of the contour pick-up unit 10 by this coefficient for outputting the product thereof. More specifically, as shown in Fig. 3, (the coefficient control unit 17) comprises the four multipliers 36_1, 36_2, 36_3 and 36_4 for selectively multiplying the contour component HE, which has been sampled by said contour pick-up unit 10 and input by way of the input terminal 34, by the coefficients 1/8, 1/4, 1/2 and 1 for outputting of the product thereof, four AND gates, 38_1, 38_2, 38_3 and 38_4 respectively connected to the output sides of the four multipliers 36_1, 36_2, 36_3 and 36_4 for using the signal decoded by the decoder 32 as gate control signal, and the OR gate 40 connected to the output sides of the four AND gates, 38_1, 38_2, 38_3 and 38_4; wherein the

contour component is output to the adder 14 from the OR gate by way of the output terminal 42. Further, in Fig. 3, for the simplicity of illustration, the delay adjusting unit 13 interposed between the decoder 32 and the coefficient control unit 17 is omitted; as the result, in the diagram, the output terminals ①, ②, ③ and ④ are shown as if the signals were directly input to the AND gates 38_1, 38_2, 38_3 and 38_4.

The delay adjusting unit 13 delays for a predetermined time interval the output of the judging signal from the level judging unit 15 in order to respectively adjust the timing for outputting to the coefficient control unit 17 the contour component HE sampled from the input luminance signal by the contour pick-up unit 10 and the timing for inputting to the coefficient control unit 17 the judging signal from the level judging unit 15.

The adder 14 adds the luminance signal Y, which has been input to the input terminal 16 and delayed for a predetermined time interval by the delay adjusting unit 12, to the contour component output from the coefficient control unit 17 for outputting the sum to the output terminal 30 as a contour-emphasized luminance signal.

The delay adjusting unit 12 delays the output of the luminance signal Y, which has been input to the input terminal 16, for a predetermined time interval in oder to respectively adjust the timing for the input of the luminance signal, which has been input to the input terminal 16, to the adder 14 and the timing for the input of the contour component, which has been output from the coefficient control unit 17, to the adder 14.

Next, the functions of the parts shown in Fig. 2 will be explained referring to Fig. 3 too.

(1) The contour component HE is sampled from the 8-bit luminance signal, which has been input to the input terminal 16, by the contour pick-up unit 10, and the sampled contour component HE is input to the coefficient control unit 17.

(2) In Fig. 3, the decoder 32 and the coefficient control unit 17 respectively function as described in (a), (b), (c) and (d) below depending on whether the luminance level of the 8-bit signal input to the input terminal 16 corresponds to which of the four levels, i.e., [00~1F] (hexadecimal number; the same applies hereinafter), [20~3F], [40~7F] and [80~FF].

(a) Case where the luminance level of luminance signal Y is [00~1F]:

The decoder 32 interprets that the luminance level is [00~1F] on the basis of that the values of upper 3 bits of the luminance signal Y is [000], thereby outputting an H-level signal from output side ①. This output signal is delayed for a predetermined time interval by the delay adjusting unit 13 (not shown in Fig. 3) and input to the AND gate 38_1 for the electrification (i.e., being kept open) thereof. In this condition, L-level signals are output from the output sides ② through ④ of the decoder 32, so that other AND gates 38_2 through 38_4 are kept unelectrified (i.e., being kept closed).

When the AND gate 38_1 is electrified, the contour component (HE/8) multiplied by 1/8 by means of the multiplier 36_1 is input to the adder 14 by way of the AND gate 38_1, OR gate 40 and output terminal 42.

(b) Case where the luminance level of luminance signal Y is [20~3F]:

The decoder 32 interprets that the luminance level is [20~3F] on the basis of that the values of upper 3 bits of the luminance signal Y are [001] and outputs an H-level signal from the output side ②. This output signal is delayed for a predetermined time interval by means of the delay adjusting unit 13 and input to the AND gate 38_2 for the electrification thereof.

When the AND gate 38_2 is electrified, the contour component (HE/4), which has been multiplied by 1/4 by multiplier 36_2, is input to the adder 14 by way of the AND gate 38_2, OR gate 40 and output terminal 42.

(c) Case where the luminance level of luminance signal Y is [40~7F]:

The decoder 32 interprets that the luminance level is [40~7F] on the basis of that the values of upper 3 bits are [010~011] and outputs an H-level signal from the output side ③. This output signal is delayed for a predetermined time interval by means of the delay adjusting unit 13 and input to the AND gate 38_3 for the electrification thereof.

When the AND gate 38_3 is electrified, the contour component (HE/2) multiplied by 1/2 by means of the multiplier 36_3 is input to the adder 14 through the AND gate 38_3, OR gate 40 and output terminal 42.

(d) Case where the luminance level of luminance signal Y is [40~7F]:

The decoder 32 interprets that the luminance level is [40~7F] on the basis of that the values of upper 3 bits are [010~011] and outputs an H-level signal from the output side ④. This output signal is delayed for a predetermined time interval by means of the delay adjusting unit 13 and input to the AND gate 38_4 for the electrification thereof.

When the AND gate 38_4 is electrified, the contour component (HE) multiplied by 1 by means of the multiplier 36_4 is input to the adder 14 through the AND gate 38_4, OR gate 40 and output terminal 42.

(3) In Fig. 2, the adder 14 adds the contour component output from the coefficient control unit 17 to the luminance signal Y, which has been input to terminal 16 and delayed for a predetermined time interval by the delay adjusting unit, to output the sum to the output terminal 30 as a contour-emphasized luminance signal.

For instance, when the luminance level of the luminance signal is [00~1F], contour component (HE/8) is added to the luminance signal Y, and the sum (Y + HE/8) as a contour-emphasized luminance signal is output to the output terminal 30. Further, when the luminance level of the luminance signal Y are [20~3F], [40~7F] or [80~FF], contour component (HE/4), (HE/2) or (HE) is added to the luminance signal Y, and sum (Y + HE/4), (Y + HE/2) or (Y + HE) as a contour-emphasized luminance signal is output to the output terminal 30. Thus, contour emphasis matching the luminance level of luminance signal Y is available.

The embodiment described above relates to a case where the contour pick-up unit comprises a horizontal contour pick-up unit for sampling the contour component in horizontal direction from the input video signal, but the present invention is not limited to this embodiment but is also applicable to other contour pick-up units as long as they are designed to sample the contour component from input video signal. For example, the present invention is applicable to the case where a contour pick-up unit comprises a vertical contour pick-up unit designed for sampling the contour component in vertical direction or to the case

where a contour pick-up unit comprises a horizontal-vertical contour pick-up unit designed for sampling the contour component in both the horizontal and vertical directions.

The embodiment described above relates to a case where the level judging unit comprises a decoder for interpreting whether the luminance level of an input video signal corresponds to which of four luminance levels, and a coefficient control unit comprises four multipliers for multiplying the contour component sampled by means of the contour pick-up unit by any of coefficients 1/8, 1/4, 1/2 and 1 for the output of respective products, four AND gates respectively connected to the output sides of the four multipliers for using the signal interpreted by the decoder as gate signal and an OR gate connected to the output sides of the four AND gates, but the present invention is not limited to this embodiment. For example, the present invention is also applicable to a case where the level judging unit comprises a decoder for interpreting whether the luminance level of a input video signal corresponds to which of n number (n = 2 or larger integers) of levels, and coefficient control unit comprises n number of multipliers for multiplying the contour component sampled by means of the contour pick-up unit by a corresponding coefficient for outputting the product thereof, n number of AND gates respectively connected to the output sides of the n number of multipliers for using, as gate control signal, the signals interpreted by a decoder, and an OR gate connected to the output sides of the n number of AND gates.

The embodiment described above relates to a case where the level judging unit comprises a decoder, and the coefficient control unit comprises multipliers, AND gates and OR gate, but the present invention is not limited to this embodiment but applicable also to the case where the level judging unit may be anything capable of discriminating the luminance level of input video signal, and the coefficient control unit may be anything capable of selectively changing the coefficient according to the judging signal from the level judging unit, as well as for multiplying the contour component sampled by means of the contour pick-up unit by a corresponding coefficient for the output of the product thereof.

INDUSTRIAL APPLICABILITY

As described in the foregoing, the present invention relates to a contour emphasizing circuit designed for sampling contour component from input video signal, multiplying the sampled contour component by a contour emphasizing coefficient, adding the product thereof to the input video signal and outputting a contour-emphasized video signal, whereby the contour can be emphasized matching with the luminance level of the input video signal. Thus, the present invention can be used for preventing production of unnatural picture either by overemphasizing the contour of a dark picture having a low luminance level by excessively adding contour component or by under emphasizing the contour of a bright picture having a high luminance level by adding insufficient contour component.

CLAIMS

1. A contour emphasizing circuit comprising a contour pick-up unit for sampling contour component from input video signal, a level judging unit for discriminating the luminance level of said input video signal, a coefficient control unit for selectively changing coefficient according to judging signal from the level judging unit and multiplying the contour component sampled by using said contour pick-up unit by the selected coefficient to output the product thereof, and an adder for adding the contour component output from the coefficient control unit to said input video signal to output the sum as a contour-emphasized video signal.

2. A contour emphasizing circuit according to claim 1, wherein the level judging unit comprises a decoder for interpreting whether the luminance level of the input video signal corresponds to which of n number (n = 2 or larger integers) of luminance levels, and the coefficient control unit comprises n number of multipliers for multiplying the contour component sampled by using the contour pick-up unit by the coefficient corresponding to one of said n number of luminance levels for outputting the product thereof, n number of AND gates respectively connected to the output sides of the n number of multipliers for using the signal interpreted by said decoder as gate control signal, and an OR gate connected to the output sides of the n number of AND gates.

3. A contour emphasizing circuit according to claim 2, wherein the level judging unit comprises the decoder for interpreting whether the luminance level of input video signal corresponds to which of four luminance levels, and the coefficient control unit comprises four multipliers for multiplying the contour components sampled by using the contour pick-up unit by any of coefficients 1/8, 1/4, 1/2 and 1 for outputting the product thereof, four AND gates respectively connected to the output sides of the four multipliers for using the signal

interpreted by said decoder as gate control signal, the OR gate connected to the output sides of the four AND gates.

4. A contour emphasizing circuit according to claim 1, 2 or 3, wherein the contour pick-up unit comprises a horizontal contour component pick-up unit for sampling the contour component in horizontal direction from input video signal.

ABSTRACT OF DISCLOSURE

A contour emphasizing circuit which comprises a contour pick-up unit 10 for picking up a contour component HE from an input luminance signal Y, a level judging unit 15 for judging the luminance level of the input luminance signal Y, a coefficient control unit 17 for changing the coefficient in a plurality of steps depending upon a judgement signal and multiplying the contour component HE by the coefficient to output the product, and an adder 14 for adding the contour component outputted from the coefficient control unit 17 to the input luminance signal Y to output an emphasized-contour luminance signal. The coefficient to be multiplied by the contour component HE is changed in a plurality of steps depending upon the luminance level of the input luminance signal Y, and the contour component HE to be added to the input luminance signal Y is controlled to have a magnitude appropriate to the luminance level of the input luminance signal Y. As a result, the contour is emphasized according to the luminance level of the input luminance signal Y without causing excessive contour emphasis by adding a large contour component to a dark image of a small luminance level, thus preventing formation of unnatural images.

Fig. 1

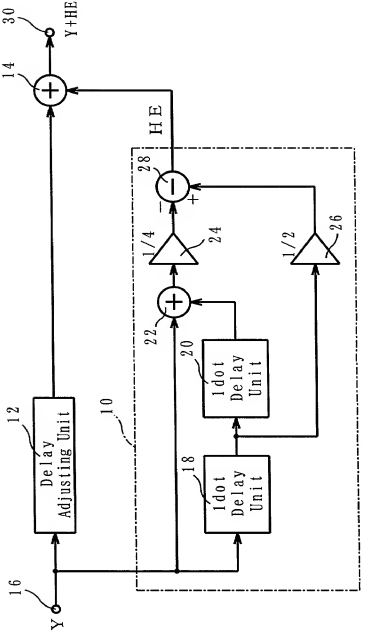


Fig. 2

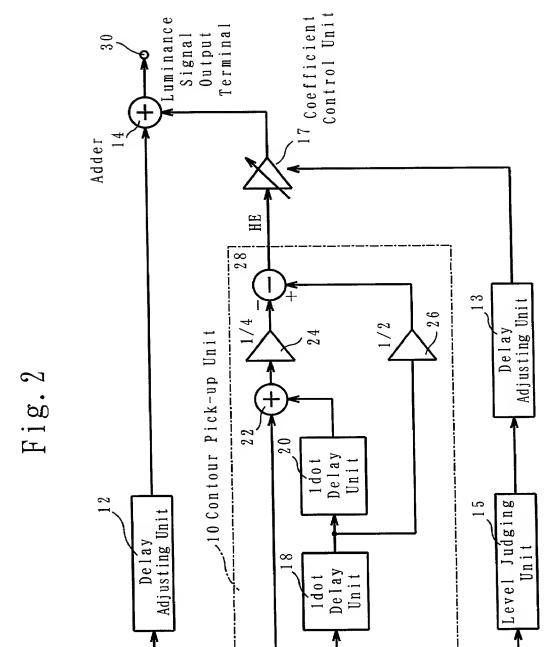
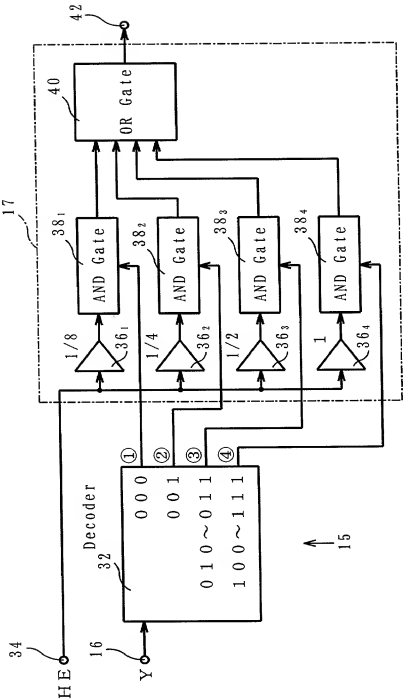

16
Luminance SignalY Input Terminal
12
Delay Adjusting Unit
10 Contour Pick-up Unit
18
1dot Delay Unit
20
1dot Delay Unit
22
1/4
24
1/2
26
28
HE
15
Level Judging Unit
13
Delay Adjusting Unit
17 Coefficient Control Unit
14
Adder
30
Luminance Signal Output Terminal

Fig. 3


42
40
OR Gate
17
38₁
38₂
38₃
38₄
AND Gate
AND Gate
AND Gate
AND Gate
1/8
1/4
1/2
1
36₁
36₂
36₃
36₄
①
②
③
④
Decoder
32
000
001
010～011
100～111
15
34
HE
16
Y

OMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY	Attorney's Docket Number
Includes Reference to PCT International Application(s))	

s below named inventor, I hereby declare that:

y residence, post office address and citizenship are as stated below next to my name,

believe I am the original, first and sole inventor (if only one name is listed below) or an original, first nd joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a atent is sought on the invention entitled:

CONTOUR EMPHASIZING CIRCUIT

he specification of which:

[X] is attached hereto.

[ ] was filed as United States application Serial No. _____
on _____
and was amended on _____ (if applicable)

[X] was filed as PCT international application Number PCT/JP98/03317
on July 24, 1998
and was amended under PCT Article 19 on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C 119:

COUNTRY (If PCT, indicate "PCT")	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 USC 119
JAPAN	213866/1997	July 25, 1997	[X] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No

hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) r PCT International Application(s) designating the United States of America that is/are listed below and, nsofar as the subject matter of each of the claims of this application is not disclosed in that/those prior pplication(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I cknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, 1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT nternational filing date of this application.

RIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. 120:

U.S. APPLICATIONS		STATUS (Check One)		
U.S. Application Number	U.S. Filing date	Patented	Pending	Abandoned

PCT APPLICATIONS DESIGNATING THE U.S.					
CT Application No.	PCT Filing Date	U.S. Serial Numbers Assigned (if any)			

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I hereby declare that all statement made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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Date January 19, 2000	Date January 19, 2000
Signature of Inventor 203: Junichi Onodera	
Date January 19, 2000	